CLAIMS

What is claimed is:

1. A method of partitioning an integrated circuit design for physical design verification including steps of:

(a) receiving as input a representation of an integrated circuit design having a number of physical design layers;

(b) receiving as input a composite run deck specifying rule checks to be performed on the integrated circuit design;

(c) partitioning the composite run deck into partitioned run decks so that the number of physical design layers referenced by each of the partitioned run decks is a minimum;

(d) parsing the representation of the integrated circuit design to filter only the physical design layers required for each of the partitioned run decks into a filtered data deck for each of the partitioned run decks; and

(e) generating as output the filtered data deck for each of the partitioned run decks.

2. The method of Claim 1 further comprising a step (f) of determining a memory size required to run each filtered data deck on a physical design verification

processor from the filtered data deck for each of the partitioned run decks.

3. The method of Claim 2 further comprising a step (g) of assigning each filtered data deck to a separate physical design verification processor according to the required memory size determined for each filtered data deck.

4. The method of Claim 3 further comprising a step (h) of performing a physical design verification concurrently for each filtered data deck on each separate physical design verification processor.

5. The method of Claim 3 wherein the each separate processor has a memory bit width of one of 32 bits and 64 bits.

6. The method of Claim 3 wherein each filtered data deck is assigned to a separate physical design verification processor having a minimum memory bit width required to run the filtered data deck.

7. The method of Claim 1 wherein the representation of the integrated circuit design is a Graphic Data System stream format file.

8. A computer program product for partitioning an integrated circuit design for physical design verification comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design having a number of physical design layers;

(b) receiving as input a composite run deck specifying rule checks to be performed on the integrated circuit design;

(c) partitioning the composite run deck into partitioned run decks so that the number of physical design layers referenced by each of the partitioned run decks is a minimum;

(d) parsing the representation of the integrated circuit design to filter only the physical design layers required for each of the partitioned run decks into a filtered data deck for each of the partitioned run decks; and

(e) generating as output the filtered data deck for each of the partitioned run decks.

9. The computer program product of Claim 8 further comprising a step (f) of determining a memory size required to run each filtered data deck on a

physical design verification processor from the filtered data deck for each of the partitioned run decks.

10. The computer program product of Claim 9 further comprising a step (g) of assigning each filtered data deck to a separate physical design verification processor according to the required memory size determined for each filtered data deck.

11. The computer program product of Claim 10 further comprising a step (h) of performing a physical design verification concurrently for each filtered data deck on each separate physical design verification processor.

12. The computer program product of Claim 10 wherein the each separate processor has a memory bit width of one of 32 bits and 64 bits.

13. The computer program product of Claim 10 wherein each filtered data deck is assigned to a separate physical design verification processor having a minimum memory bit width required to run the filtered data deck.

14. The computer program product of Claim 8 wherein the representation of the integrated circuit design is a Graphic Data System stream format file.